

FORM PTO-1449	SERIAL NO. <i>10/813, 455</i> <i>Not Yet Assigned</i>	CASE NO. 10519-118
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE <i>3/29/04</i> <i>Herewith</i>	GROUP ART UNIT <i>Not Yet Assigned</i> <i>2818</i>
(use several sheets if necessary)	APPLICANT(S): Vyvoda et al	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
<i>TP</i>	A1	4,799,196	01/1989	Takemae		
	A2	5,029,125	07/1991	Sciupac		
	A3	5,249,282	09/1993	Segers		
	A4	5,285,323	02/1994	Hetherington et al.		
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	A6	5,699,317	12/1997	Sartore et al.		
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	A8	5,812,418	09/1998	Lattimore et al.		
	A9	5,818,748	10/1998	Bertin et al.		
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	A11	5,856,221	01/1999	Clementi et al.		
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EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
EXAMINER	<i>Trong Phan</i>	DATE CONSIDERED <i>8/4/04</i>

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
<i>TP</i>	A35	"MultiMediaCard System Specification Version 2.2 Official Release," pages 10, 12, and 14, January 2000.
	A36	"A 10ns Read and Write Non-Volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell," Scheuerlein et al., ISSCC 2000/Session 7/TD: Emerging Memory & Device Technologies/Paper TA 7.2, 4 pages, February 8, 2000.
	A37	"A 125mm <sup>2</sup> /Gb NAND Flash Memory with 10MB/s Program Throughput," Nakamura et al., ISSCC 2002/Session 6/SRAM and Non-Volatile Memories/6.4, 10 pages (December 4, 2002).
	A38	"Three-Dimensional Memory Array and Method of Fabrication," Johan Knall, U.S. App. Serial No. 09/560,626 filed April 28, 2002.
	A39	"Method for Deleting Stored Digital Data from Write-Once Memory Device," Christopher S. Moore, Derek J. Bosch, Daniel C. Steere, J. James Tringali, U.S. Patent Application Serial No. 09/638,439 filed August 14, 2002.
	A40	"Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern under a Plurality of Memory Arrays," Roy E. Scheuerlein, U.S. Patent Application Serial No. 09/896,814 filed June 29, 2001
	A41	"Memory Devices and Methods for Use Therewith," Roger W. March, Christopher S. Moore, Daniel Brown, Thomas H. Lee, Mark G. Johnson, U.S. Patent Application Serial No. 09/748,589 filed December 22, 2000.
	A42	"Method for Reading Data in a Write-Once Memory Device Using a Write-Many File System," Christopher S. Moore, J. James Tringali, Roger W. March, James E. Schneider, Derek J. Bosch, Daniel C. Steere, U.S. Patent Application Serial No. 09/878,138 filed June 8, 2001.
	A43	"Method for Re-Directing Data Traffic in a Write-Once Memory," J. James Tringali, Christopher S. Moore, Roger W. March, James E. Schneider, Derek J. Bosch, Daniel C. Steere, U.S. Patent Application Serial No. 09/877,691 filed June 8, 2001.
	A44	"Memory Device and Method for Storing and Reading Data in a Write-Once Memory Array," Christopher S. Moore, James E. Schneider, J. James Tringali, Roger W. March, U.S. Patent Application Serial No. 09/877,720 filed June 8, 2001.
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	A47	"Modular Memory Device," J. James Tringali, P. Michael Farmwald, Thomas H. Lee, Mark G. Johnson, Derek J. Bosch, U.S. Patent Application Serial No. 09/638,334 filed August 14, 2000.
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